AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for optimizing memory bandwidth, comprising:

requesting data associated with a first address;

obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor;

storing the data associated with the first address and data associated with the consecutive address in a temporary data storage area;

requesting data associated with a second address; and

determining whether the data associated with the second address is stored in the temporary data storage area ~~through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address.

2. (Original) The method of claim 1, wherein the method operation of obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor includes,

completing the obtaining the data associated with the first address and data associated with a consecutive address in one clock cycle associated with the microprocessor.

3. (Currently Amended) The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the temporary data storage area ~~buffer through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address includes,

comparing the most significant bits of the signal to corresponding most significant bits of a previous signal, the most significant bits being all bits except first and second least significant bits; and

if the most significant bits of the signal are equal to the corresponding most significant bits of the previous signal, then the method includes,

accessing the data in the temporary data storage area according to the first and second least significant bits.

4. (Currently Amended) The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the temporary data storage area ~~buffer through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address includes,

comparing the most significant bits of the signal to corresponding most significant bits of a previous signal; and

if the most significant bits of the signal are not equal to the corresponding most significant bits of the previous signal, then the method includes,

fetching the data associated with the second address from the memory region; and

fetching consecutive data associated with the second address from the memory region.

5. (Currently Amended) The method of claim 4, further comprising:

determining an amount of consecutive data to fetch according to a value associated with ~~the~~ first and second least significant bits of the signal.

6. (Currently Amended) A method for efficiently executing memory reads based on a read command issued from a central processing unit (CPU), comprising:

requesting data associated with a first address in memory in response to receiving the read command;

storing the data associated with the first address in a buffer;

storing data associated with a consecutive address relative to the first address in the buffer, the storing occurring prior to the CPU being capable of issuing a next command following the read command;

determining if a next read command corresponds to the data associated with the consecutive address according to corresponding most significant bits of the read command and the next read command; and

if the next read command corresponds to the data associated with the consecutive address, the method includes,

obtaining the data from the buffer according to least significant bits of the next read command.

7. (Original) The method of claim 6, further comprising:

if the next read command does not correspond to the data associated with the consecutive address, the method includes,

storing data associated with the next read command in the buffer; and

storing data having a consecutive address to the data associated with the next read command in the buffer.

8. (Original) The method of claim 6, wherein the method operation of determining if a next read command corresponds to the data associated with the consecutive address includes,

comparing a signal associated with the read command to a signal associated with the next read command.

9. (Original) The method of claim 6, wherein the method operation of storing data associated with a consecutive address relative to the first address in the buffer includes,

issuing a read store select signal; and

directing the data to a storage location of the buffer according to the read store select signal.

10. (Currently Amended) The method of claim 6, wherein the method operation of obtaining the data from the buffer includes,

determining a location of the data in the buffer through a data select signal corresponding to the least significant bits of the next read command.

11. (Currently Amended) A memory controller, comprising:

logic for requesting a read operation from memory;

logic for generating an address for the read operation;

logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage; and

logic for determining if a request for data associated with a next read operation is for the data associated with the consecutive address in the temporary storage according to corresponding most significant bits associated with requesting the read and the next read operation.

12. (Currently Amended) The memory controller of claim 11, wherein the logic for determining if a request for data associated with a next read operation is for the data associated with the consecutive address in the temporary storage includes,

a comparator configured to compare the corresponding most significant bits of a signal corresponding to the request for data associated with a next read operation with a signal corresponding to the address for the read operation.

13. (Original) The memory controller of claim 11, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage is configured to issue a signal for distributing the data associated with the address and the data associated with the consecutive address in the temporary storage.

14. (Original) The memory controller of claim 11, wherein the logic for requesting a read operation from memory originates from a microprocessor.

15. (Original) The memory controller of claim 14, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage includes,

completing the storing prior to the microprocessor being capable of issuing any command following the read operation.

16. (Currently Amended) An integrated circuit, comprising:

circuitry for issuing a command;

memory circuitry in communication with the circuitry for issuing the command, the memory circuitry including,

a random access memory (RAM) core circuitry;

a memory controller configured to issue a first request for data associated with an address of the RAM, the memory controller further configured to issue a second request for data associated with a consecutive address to the address; and

a buffer in communication with the memory controller, the buffer configured to store the data associated with the address and the consecutive address in response to the respective requests for data, the data associated with the address and the consecutive address being stored prior to a next command being issued, wherein the memory controller includes circuitry configured to determine whether the second request is for the data associated with the consecutive address <u>according to corresponding most significant bits associated with the first request and the second request</u>.

17. (Currently Amended) The integrated circuit of claim 16, wherein the memory circuitry further comprises:

a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and

a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address, <u>wherein the second multiplexer is not coupled to the RAM</u>.

18. (Original) The integrated circuit of claim 16, wherein the memory controller includes a comparator configured to compare a signal corresponding to the first request with a signal corresponding to the second request to determine if the data associated with the second request is in the buffer.

19. (Original) The integrated circuit of claim 16, wherein the RAM core circuitry is configured as synchronous dynamic random access memory (SDRAM) circuitry.

20. (Currently Amended) The integrated circuit of claim 16, wherein the memory controller includes selection and storage logic configured to enable one of distribution of the data associated with the address and the consecutive address into the buffer, and access to the data associated with the address and the consecutive address from the buffer, the access to the data being performed according to least significant bits of the second request.

21. (Currently Amended) A device, comprising:

a graphics processing unit (GPU);

a memory region in communication with the GPU over a bus,

the memory region configured to receive a read command from the GPU, the memory region including,

a read buffer for temporarily storing data; and

a memory controller in communication with the read buffer, the memory controller configured to issue requests for one of fetching data in memory having an address associated with the read command and fetching data in memory associated with a consecutive address to the address according to least significant bits of the request for fetching data in memory, in response to receiving a read command from the GPU, wherein the requests cause the data associated with the consecutive address to be stored in the read buffer prior to the GPU issuing a next command after the read command.

22. (Original) The device of claim 21, wherein the memory region includes,

a first multiplexer configured to distribute the data having the address and the data associated with the consecutive address into the buffer; and

a second multiplexer configured to select the data associated with the consecutive address when the next command is for the data associated with the second address.

23. (Original) The device of claim 21, wherein the memory controller further includes,

selection and storage logic configured to enable one of distribution of the data having the address and the data associated with the consecutive address

into the buffer, and access to the data having the address and the data associated with the consecutive address from the buffer.

24. (Original) The device of claim 21, wherein the memory controller further includes, a comparator configured to compare a signal corresponding to the read command with a signal corresponding to a next read command to determine if data associated with the next read command is in the buffer.

25. (Original) The device of claim 21, wherein the device is a portable handheld electronic device.

26. (Original) The device of claim 21, further comprising:

a display screen configured to display image data.